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[METHOD AND CIRCUIT FOR DYNAMIC READ MARGIN CONTROL OF A MEMORY ARRAY]

Abstract

A method and circuit for adjusting the read margin of a self-timed memory array. The electronic circuit, including: a memory cell array including a sense amplifier self-timed decode circuit adapted to set a base read time delay of the memory cell array; and a read delay adjustment circuit coupled to the memory cell array, the read delay adjustment circuit adapted to adjust the base read time delay of the memory array based on an operating frequency of the memory cell array.